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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,674	03/18/2004	William F. Clark JR.	BUR920030158US1	2673

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FREDERICK W. GIBB, III
GIBB INTELLECTUAL PROPERTY LAW FIRM, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,674	CLARK ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-9,13 and 14* is/are rejected.

7)☒ Claim(s) *4-6,10-12 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 3, 7, 8, 9, 13, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Cohen (United States Patent Application Publication No. US 2005/0040444 A1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

4. In reference to claim 1, Cohen (United States Patent Application Publication No. US 2005/0040444 A1) discloses a device which meets the claim. Figure 22 discloses a semiconductor structure having at least one fin-type field effect transistor (FinFET). The semiconductor structure in figure 22 comprises a substrate and two fins (11) which extend from it. A first gate dielectric (12) covers opposing sides of the first fin. A second gate dielectric (15) covers opposing sides of the second fin. The first gate dielectric (12) has a first thickness and the second gate dielectric (15) has a second thickness which is different from the first thickness (p. 4, paragraph 72).

5. In reference to claim 2, it is understood that the semiconductor structure shown in figure 22 is one of many formed on the same substrate and that the first and second fins are to be utilized in different transistors in the substrate. The examiner notes the limitation with regard to the different voltage requirements for the different transistors. However this has not been given any patentable weight since no structural limitation has been imposed.

6. With regard to claim 3, Cohen (United States Patent Application Publication No. US 2005/0040444 A1) discloses a device which meets the claim. Figure 22 discloses a semiconductor structure having at least one fin-type field effect transistor (FinFET). The semiconductor structure in figure 22 comprises a substrate having fins (11) which extend from it. Gate dielectrics (12, 15) cover the fins. The gate dielectrics (12, 15) have different thicknesses (p. 4, paragraph 72). The fins are utilized in at least one multiple-fin transistor.

7. In reference to claim 7, Cohen (United States Patent Application Publication No. US 2005/0040444 A1) discloses a device which meets the claim. Figure 22 discloses a semiconductor structure having at least one fin-type field effect transistor (FinFET). The semiconductor structure in figure 22 comprises a substrate and two fins (11) which extend from it. Each of the fins comprises a central channel region and source and drain regions on opposite ends of the channel region. A first gate dielectric (12) covers opposing sides of the channel region of the first fin. A second gate dielectric (15) covers opposing sides of the channel region of the second fin. The first gate dielectric (12) has a first thickness and the second gate dielectric (15) has a second thickness which is different from the first thickness (p. 4, paragraph 72).

8. In reference to claim 8, it is understood that the semiconductor structure shown in figure 22 is one of many formed on the same substrate and that the first and second fins are to be utilized in different transistors in the substrate. The examiner notes the limitation with regard to the different voltage requirements for the different transistors. However this has not been given any patentable weight since no structural limitation has been imposed.

9. In reference to claim 9, Cohen (United States Patent Application Publication No. US 2005/0040444 A1) discloses a device which meets the claim. Figure 22 discloses a semiconductor structure having at least one fin-type field effect transistor (FinFET). The semiconductor structure in figure 22 comprises a substrate and fins (11) which extend from it. Each of the fins comprises a central channel region and source and drain regions on opposite ends of the channel region. Gate dielectrics (12, 15) cover the fins.

The gate dielectrics (12, 15) have different thicknesses (p. 4, paragraph 72). The fins are utilized in at least one multiple-fin transistor.

10. In reference to claim 13, Cohen (United States Patent Application Publication No. US 2005/0040444 A1) discloses a device which meets the claim. Figure 22 discloses a semiconductor structure having a fin-type field effect transistor (FinFET). The semiconductor structure in figure 22 comprises a substrate and two fins (11) which extend from it. A first gate dielectric (12) covers opposing sides of the first fin. A second gate dielectric (15) covers opposing sides of the second fin. The first gate dielectric (12) has a first thickness and the second gate dielectric (15) has a second thickness which is different from the first thickness (p. 4, paragraph 72). It is understood that the semiconductor structure shown in figure 22 is one of many formed on the same substrate and that the first and second fins are to be utilized in different transistors in the substrate. The examiner notes the limitation with regard to the use of complementary FinFETs. However Cohen makes it clear that FinFETs may be implemented as complementary transistors (p. 1, paragraph 4).

11. In reference to claim 14, Cohen (United States Patent Application Publication No. US 2005/0040444 A1) discloses a device which meets the claim. Figure 22 discloses a semiconductor structure having a fin-type field effect transistor (FinFET). The semiconductor structure in figure 22 comprises a substrate and fins (11) which extend from it. Gate dielectrics (12, 15) cover the fins. It is understood that the fin-type field effect transistor (FinFET) shown in figure 22 is one of many formed on the same substrate and that the first and second fins are to be utilized in different transistors in

the substrate. A first type of transistor has gate dielectrics (12) having a first thickness. A second type of transistor has gate dielectrics (15) having a second thickness. The first thickness and the second thickness are different from each other (p. 4, paragraph 72). The fins are utilized in multiple-fin transistors.

Allowable Subject Matter

12. Claims 4-6, 10-12, and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware if any prior art which suggests or renders obvious double gate finfet devices having two fins with gate dielectric layers on each of the opposing sides of the fins which are different in thickness which utilize multiple dielectric layers to achieve a greater gate dielectric thickness.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ